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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,752	11/17/2003	Chun Chen	400.235US01	3378

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/714,752	CHEN ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) *18-87* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/26/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-78, drawn to method, classified in class 438, subclass 201.

II. Claims 79-87, drawn to device, classified in class 257, subclass 314.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product invention II can be made by another and materially different process. For example, a polysilicon with an ion implanted top layer can be formed by selective deposition instead of selectively implanting ions into one or more regions of polysilicon and etching the polysilicon to removed the non-implanted region of polysilicon.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

6. The method invention I of this application contains claims directed to the following patentably distinct species of the claimed invention:

Ia. Species Ia, claims 1-17, drawn to a method of fabricating a source interconnect to a memory cell including removing a portion of the exposed portion of the layer of dielectric material to expose the source region, removing the first mask layer; forming a layer of polysilicon overlying the layer of dielectric material and in contact with the exposed source region; forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the source region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of popysilicon and an non-implanted portion of the layer of polysilicon.

Ib. Species Ib, claims 18-31, drawn to a method of fabricating a local interconnect comprising depositing a layer of silicon containing material over the dielectric layer, selectively implanting ions in one or more regions of the layer of silicon-containing material over the one or more trenches; and wet etching the layer of silicon containing material to remove the non-implanted regions of the layer of silicon-containing material to form one or more local interconnect line in the one or more trenches.

Ic. Species Ic, claims 32-44, method of fabricating a memory array comprising forming a plurality of word line gate stacks, each containing a plurality of memory cell; forming a dielectric layer having one or more trenches; depositing a layer of polysilicon over the dielectric layer, selectively implanting ions in one or more regions of the layer of polysilicon over the trenches, and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local interconnect lines in the one or more trenches.

Id. Species Id, claims 45-59, drawn to a method of fabricating a floating gate memory cell comprising forming a dielectric spacer over a gate stack having at least one or more contact holes to the source region of the memory cell; depositing a layer of polysilicon overlying the dielectric spacer layer to contact the source region of the memory cell through the at least one contact hole of the dielectric spacer; selectively implanting ions in one or more selected regions of the layer of polysilicon; and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form at least one polysilicon local interconnect from the selected regions of the layer of polysilicon.

Ie. Species Ie, claims 60-67, drawn to a method of forming an array of floating gate memory cells comprising forming dielectric spacer layer over the word line gate stack, removing a portion of the dielectric spacer layer to define trenches exposing source regions, wherein each trench exposes a plurality of source regions; depositing a third polysilicon layer over the dielectric spacer

layer, where the third polysilicon layer fills the trenches; selectively implanting ions in one or more regions of the third polysilicon layer; and wet etching the third polysilicon layer to remove the non-implanted regions of the third polysilicon layer to form one or more polysillicon source local interconnect lines in the one or more trenches.

If. Species If, claims 68-71, drawn to a method of forming a floating gate memory comprising forming a spacer dielectric layer overlying the plurality of word line gate stacks having one or more trenches, where the one or more trenches expose one or more source regions of the plurality of memory cells, depositing a layer of polysilicon overlying the spacer dielectric layer, selectively implanting ions in one or more regions of the layer of polysilicon, and wet etching the layer of polysilicon to remove the non-implanted regions of the layer of polysilicon to form one or more polysilicon local intetconnect lines in the one or more trenches.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

7. The device invention II of this application contains claims directed to the following patentably distinct species of the claimed invention:

IIa. Species IIa, claims 72-78, drawn to a floating gate memory cell comprising a tunnel dielectric layer formed overlying a semiconductor substrate;

a drain region formed in a semiconductor substrate adjacent a first side of the tunnel dielectric layer; a source region formed in a semiconductor substrate adjacent a second side of the tunnel dielectric layer, a floating-gate layer formed overlying the tunnel dielectric layer, an intergate dielectric layer formed overlying the floating-gate layer, a control gate layer formed overlying the intergate dielectric layer; a first contact coupled to the source region, and

wherein the first contact comprises a polysilicon layer with an ion implanted top layer.

IIb. Species IIb, claims 79-87, drawn to a memory device comprising an array of floating-gate memory cells, wherein the array comprises a plurality of rows of memory cells, each row coupled to a word line; a plurality of columns of memory cells, each columns coupled to a bit line; a plurality of array source interconnects, each interconnect coupled to source regions of at least a portion of a row of memory cells; and a plurality of drain contacts, each drain contact coupled between a drain region of a memory cell and a bit line; and wherein each array source interconnect comprises a polysilicon layer with an ion implanted top layer. where each array source interconnect is in contact with its associated source regions.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

8. Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

9. During a telephone conversation with Andrew Walseph on 05/11/05 a provisional election was made without traverse to prosecute the invention of species Ia, claims 1-17. Affirmation of this election must be made by applicant in replying to this Office action. Claims 18-87 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to non-elected inventions.

10. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Oath/Declaration

11. Oath/Declaration filed on 01/17/2003 has been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 3, 7 and 17 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

► With respect to claim 3, term "and/or" renders the claim indefinite. It is not clear what "patterning the first or second mask layer with the same pattern" means. In addition, it is not how the first and second mask layer can be patterned with the same pattern. It is not clear how a pattern can be defined as the same pattern.

► With respect to claim 7, " wherein selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect further comprises selectively wet etching the layer of polysilicon to

preferentially remove the implanted portion, thereby forming the source interconnect" renders the claim indefinite. It is not clear how selectively etching the layer of polysilicon preferentially remove the non-implanted portion can preferentially remove the implanted portion.

► With respect to claim 17, "patterning first and second mask layers further comprises patterning first and second mask layers to additionally expose a portion of the layer of dielectric over at least the drain region" renders the claim indefinite. It is not clear how the second mask layer can expose a portion of the layer of dielectric when the second mask layer is formed overlying the layer of polysilicon wherein the layer of polysilicon overlying the layer of the dielectric.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-9, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim [US 6,001,685] in view of Wu et al. [US 6,309,975].

► With respect to claims 1, 5-8 and 14, Kim (figs 6's and col. 1-7) discloses a method of fabricating a source interconnect to a memory cell comprising:

forming a layer of dielectric material (28/29/30, fig 6B) overlying a gate stack (23/24/25), a source region (26) and a drain region (28) of the memory cell;

forming a first mask layer (31, fig 6B) overlying the layer of dielectric material;

patterning the first mask layer (31, fig 6B) to expose a portion of the layer of dielectric material over at least the source region;

removing a portion of the exposed portion of the layer of dielectric material to expose the source region (26, fig 6C);

removing the first mask layer (31, fig 6C);

forming a layer of polysilicon (32, fig 6C) overlying the layer of dielectric material and in contact with the exposed source region; and

selectively etching the layer of polysilicon thereby forming the source interconnect (32', fig 6D).

Kim does not teach said selectively etching the layer of polysilicon comprising: forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the source region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect ***[claim 1]***, wherein said implanting ion comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon and silicon ***[claim 14]***, wherein said selectively etching the layer of polysilicon comprises selectively wet etching the layer of polysilicon ***[claims 5 and 7]*** with TMAH ***[claim 6]*** or KOH ***[claim 8].***

However, Wu et al (figs 21-23, col. 8-11, 34-40 and 47-48) teaches forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over an active region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the polysilicon interconnect, wherein said implanting ion comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon and silicon, wherein said selectively etching the layer of polysilicon comprises selectively wet etching the layer of polysilicon with TMAH or KOH.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Kim by using the second mask, implanting ions and selectively etch as being claimed, per taught by Wu et al., to provide a better control in selectively etching the layer of polysilicon to form the source interconnection.

► With respect to claim 2, Kim (col. 6 lines 16-30) disclose forming the first and/or second mask (first mask 31) with a photoresist.

► With respect to claim 4, the layer of polysilicon overlying the dielectric material and in contact with the exposed source region in the process of Kim in view of Wu et al would be conductively doped for functioning as conductor polysilicon for the source interconnection.

► With respect to claim 9, the layer of polysilicon overlying the layer of dielectric material would be a layer of silicon containing layer.

► With respect to claims 12-13, the claimed range of ion dosage level of implanting ion is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

► With respect to claim 15, removing the first and/or second mask in the process of Kim in view of Wu et al would comprise stripping the first and/or second mask.

► With respect to claim 16, Kim (col. 6 lines 26-35) discloses removing a portion of the exposed portion of the layer of dielectric material to expose the source region comprises anisotropically etching the exposed portion of the layer of dielectric material.

► With respect to claim 17, Kim (fig 6B-C) shows patterning the first mask layer comprising patterning the first mask layer to additionally expose a portion of the layer of dielectric over at least the drain region (26').

14. Claims 1-2 and 4-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenq et al. [US 6,159,788] in view of Wu et al [US 6,309,975].

► With respect to claims 1, 5-8 and 14, Jenq et al (figs 1-5 and col. 1-10) discloses a method of fabricating a source interconnect to a memory cell comprising:

forming a layer of dielectric material (36, fig 2) overlying a gate stack (14/16/18/20), a source region (30) and a drain region (28) of the memory cell;

forming a first mask layer overlying the layer of dielectric material (col. 6 lines 1-7);

patterning the first mask layer (having the first mask pattern with an opening over the source region 30, col. 6 lines 1-7) to expose a portion of the layer of dielectric material over at least the source region;

removing a portion of the exposed portion of the layer of dielectric material to expose the source region (fig 3, col. 6 lines 1-16);

removing the first mask layer (col 6 lines 28-29);

forming a layer of polysilicon (42, fig. 4) overlying the layer of dielectric material and in contact with the exposed source region; and

selectively etching the layer of polysilicon thereby forming the source interconnect (44, fig 5).

Kim does not teach said selectively etching the layer of polysilicon comprising: forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the source region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect ***[claim 1]***, wherein said implanting ion comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon and silicon ***[claim 14]***, wherein said selectively etching the layer of polysilicon comprises selectively wet etching the layer of polysilicon ***[claims 5 and 7]*** with TMAH ***[claim 6]*** or KOH ***[claim 8].***

However, Wu et al (figs 21-23, col. 8-11, 34-40 and 47-48) teaches forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over an active region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the polysilicon interconnect, wherein said implanting ion comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon and silicon, wherein said selectively etching

the layer of polysilicon comprises selectively wet etching the layer of polysilicon with TMAH or KOH.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Jenq by using the second mask, implanting ions and selectively etch as being claimed, per taught by Wu et al., to provide a better control in selectively etching the layer of polysilicon to form the source interconnection.

► With respect to claim 2, Jenq et al (col. 6 lines 27-29) disclose forming the first and/or second mask (first mask) with a photoresist.

► With respect to claim 4, Jenq et al (col. 6 lines 30-45) discloses forming the layer of polysilicon overlying the layer of the dielectric material and in contact with the exposed source region wherein the layer of polysilicon is conductively doped.

► With respect to claim 9, the layer of polysilicon overlying the layer of dielectric material would be a layer of silicon containing layer.

► With respect to claim 10, Jenq et al (figs 2-3 and col 6 lines 1-7) disclose patterning the first mask layer comprises patterning the first mask layer to expose a portion of the layer of the dielectric over the source region and a portion of the gate stack.

► With respect to claim 11, in combination of process of Jenq et al in view of Wu et al, to form the source interconnect (44) overlying the source region (30) and a portion of the gate stack, patterning the second mask would expose a portion of the layer of polysilicon over the source region and a portion of the gate stack.

► With respect to claims 12-13, the claimed range of ion dosage level of implanting ion is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

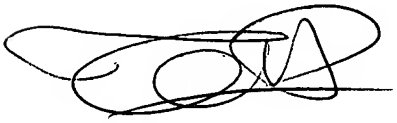
► With respect to claim 15, removing the first and/or second mask in the process of Jenq et al in view of Wu et al would comprise stripping the first and/or second mask.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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